IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Charles Dennison	Group Art Unit:	
Serial No.:	10/652,631		
Filed:	August 29, 2003	Examiner:	
For:	Lower Electrode Isolation In A Double-Wide Trench And Method Of Making Same	Atty. Dkt. No.:	ITO.0539D1US (P10144D)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicant submits the references listed on the attached form PTO 1449 together with any required copies of such references.

This statement is being filed within three months of the filing date of the application. Please apply any charges or credits to Deposit Account No. 20-1504 (ITO.0539D1US).

Respectfully submitted,

Date: 10/30/03

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Date of Deposit: 10-31-03
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
Sherry Tipton
Sherry Tipton

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
ITO.0539D1US (P10144D)	10/652,631
APPLICANT(S): CHARLES DENNISON	
FILING DATE: August 29, 2003	GROUP ART UNIT:

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	A.						
	B.						
	C.						
	D.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	E.							
	F.							
	G.							
	H.							

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	I.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C.., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Jeong, U.I., Jeong, H.S. and Kim, Kinam, "Completely CMOS-Compatible Phase-Change Nonvolatile RAM Using NMOS Cell Transistors," presented at 2003 19th IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, California, February 26-20, 2003
	J.	Ha, Y.H., Yi, J.H., Horii, H., Park, J.H., Joo, S.H., Park, S.O., Chung, U-In and Moon, J.T., "An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003
	K.	Hwang, Y.N., Hong, J.S., Lee, S.H., Ahn, S.J., Jeong, G.T., Koh, G.H., Oh, J.H., Kim, H.J., Jeong, W.C., Lee, S.Y., Park, J.H., Ryoo, K.C., Horii, H., Ha, Y.H., Yi, J.H., Cho, W.Y., Kim, Y.T., Lee, K.H., Joo, S.H., Park, S.O., Chung, U.I., Jeong, H.S. and Kim, Kinam, "Full Integration and Reliability Evaluation of Phase-change RAM Based on 0.24 mm-CMOS Technologies," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003
	L.	Horii, H., Yi, J.H., Park, J.H., Ha, Y.H., Baek, I.G., Park, S.O., Hwang, Y.N., Lee, S.H., Kim, Y.T., Lee, K.H., Chung, U-In and Moon, J.T., "A Novel Cell Technology Using N-doped GeSbTe Films for Phase Change RAM," presented at IEEE 2003 Symposium on VLSI Technology, Kyoto, Japan, June 12-14, 2003
	M.	
	N.	
	O.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.